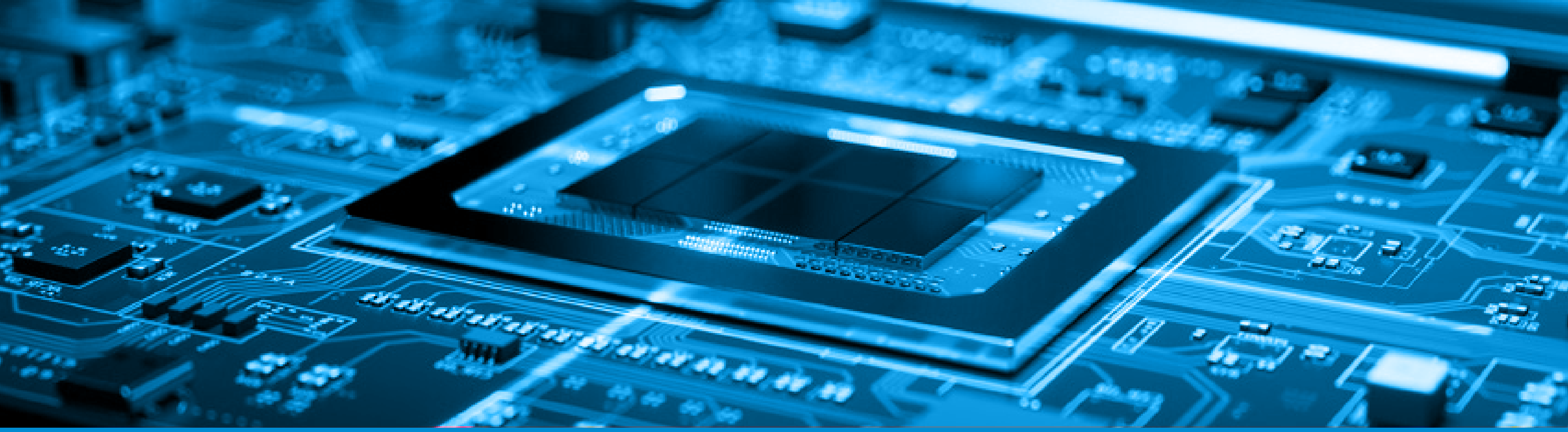

Real Time X-ray Analysis of Void Formation and Dynamics In QFN Devices During Reflow

By Sandeep Kullar, Christopher Rand, and Evstatin Krastev

Abstract

High powered devices require electrical circuits with good thermal conductance and minimal voiding, to maintain long life time and optimum performance throughout. One example is the Quad Flat No-leads (QFN) package. QFN devices electrically connect an integrated circuit to Printed Circuit Boards (PCB's). QFN devices, being surface mount technology (SMT) are placed onto PCB's, that are pre-printed with solder paste. These solder pastes require their own unique thermal profiles to achieve optimum performance. Usually, the initial profiles are provided by the solder paste suppliers, and fine-tuned at the SMT manufacturers facility. Common defects found within QFN devices include solder bridges, open connections and large solder voiding. Large solder voiding can occur if an unsuitable solder paste is applied, and/or if the thermal reflow profile being used is not optimized. Using conventional reflow ovens, it is not possible to examine void formation and their dynamics in real-time. The goal of this study is to discuss a new X-ray technique that permits monitoring reflow process in real time and gain basic understanding of void formation dynamics for QFN devices utilizing several types of solder pastes. The equipment used is called X-ray Reflow Simulator. Basically, it is a small reflow oven that fits inside the X-ray machine to observe the reflow process in real time. It has the capability to follow pre-set heating and cooling profile to emulate the processes within the SMT oven.

Key words: X-ray inspection, X-ray Reflow Simulator, 2DX, MXI, AXI, Computer Tomography, CT, 2D, 3D, Quad Flat No-leads (QFN), BGA, SMT, PCBA, Voiding, X-ray.

Introduction

There is an increasing demand for the use of Quad Flat No Lead (QFN) packages within the electronics industry. QFN's consist of an integrated circuit, a copper lead frame substrate and a thermally conductive pad. Land pads located around the perimeter of the package connect the device to the PCB. QFN devices have grown more popular with advancing technology. This is because they are low cost, have great thermal and electrical properties and allow for thinner products to be manufactured, due to their small size.

The quality of the central pad connection to the PCB is crucial for removing heat from the component. If this pad is damaged or contains excessive amounts of voiding, this will affect the thermal efficiency and can cause the device to overheat and fail. The central pad is located on the underside of the package, and therefore, once mounted cannot be inspected optically. X-ray is the best non-destructive inspection method to check quality of this joint, and the smaller planar connections around the edge.

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Background

X-ray Technology

The 2D X-ray inspection has become a critically important tool within the test and inspection regime of the electronics design, development and manufacturing groups [1-10]. The reason is that it provides the only means of inspecting optically hidden solder joints as well as looking inside microelectronics packages in a completely non-destructive fashion. The only alternative is the mechanical cross sectioning. While the mechanical cross-section technique is widely used for failure analysis and development purposes, it has a major disadvantage – the expensive device or printed circuit board (PCB) is being cut through and in this way destroyed without any chance for repair.

The technology within X-ray inspection systems has massively improved over recent years, and acquiring a high resolution 2D image for analysis can be achieved in seconds, from the point of sample loading [1]. The ability to be able to do this relates to significant developments in the X-ray inspection technology in recent years. X-ray sources with submicron feature recognition down to 0.1 micron (100 nanometers) and very high power up to 20 Wats are now available. These novel X-ray sources do not defocus the beam and deliver submicron resolution up to the full 20W of power. New advanced CMOS flat panel detectors provide very low noise, extremely high sensitivity and resolution. Running at high acquisition rates of 30 fps these provide crystal clear and extremely sharp 6.7 Megapixel images with 65,000 levels of grey.

Digital image processing functions (filters) enhance the X-ray images quickly making it much easier to spot the finest defects. The use of filter pipelines, which is a linear chain of individual filters, effectively enhance image contrast and sharpness simultaneously. Figure 1 below displays a digitally enhanced X-ray image of a defective QFN device.

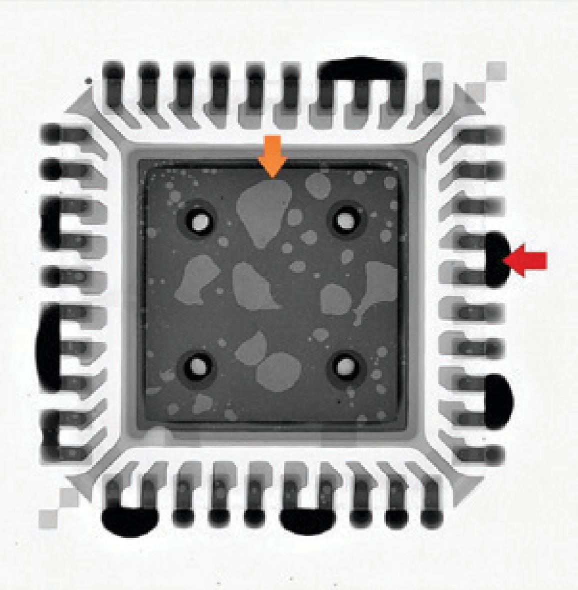

Figure 1. High resolution 2D X-ray image of a defective QFN. Red arrow highlighting solder bridging between pads, and orange arrow highlighting large solder voiding.

Defects such as solder bridging between pads (highlighted with a red arrow on Figure 1), and large voiding (highlighted with an orange arrow on Figure 1) are easily detected. Defects of this kind often occur if there is excessive solder paste applied to the PCB, and if the thermal profile and/or solder paste used are not suitable. Minimising voiding within solder during the reflow process can be challenging; and therefore, gaining an insight on solder behaviour during the heating process is crucial.

Voiding Analysis

Once solder reflow has been achieved, the next step is to check the quality of the connection and a significant part of this is the measurement of solder voiding. The brighter patches on Figure 2 represent regions of lower density corresponding to solder voids. These are outlined in color on Figure 2. The darker areas represent regions of higher density where there is a sufficient solder amount.

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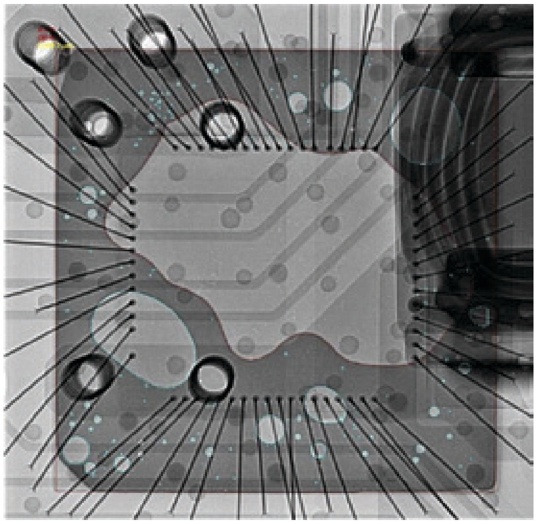

Figure 2. 2D X-ray image displaying voiding analysis on a QFN device. All voids detected have been outlined in color. The blue outlines represent voids within acceptable limit and red outline represents a void outside the acceptable limit.

Advanced X-ray algorithms allow the voiding to be calculated easily and quickly (just couple of mouse clicks) using manual, semi-auto or full auto modes. For accurate results, each pixel on the picture is analysed to determine if it is part of a void or not.

The QFN device on Figure 2 is a part of a very complex PCB assembly. On the 2D image there are wire bonds, multiple via holes, and a large component to the top right of the image. All these are obstructing the QFN pad of interest. For a further in-depth analysis, and to isolate the layer of interest where the QFN pad voiding are located, 3D computer tomography techniques are employed. These include µCT and Large Board X-plane CT.

Computer Tomography

Computer Tomography is a powerful non-destructive inspection technique used widely in the electronics industry, especially for the analysis of multi-layered devices and joint interconnections. The CT technique permits different layers/ slices of the device to be isolated and examined individually, so practically providing an electronic, or virtual, cross-sectioning within the sample. The benefits of an ‘electronic cross-section’ compared to traditional mechanical cross-sectioning are many. These include that the electronic cross-sectioning is reversible, and you cannot over polish and go too far into the sample. The cutting plane can be positioned in any orientation within the 3D space of the CT model, and no additional defects are introduced or existing defects concealed compared with the process of mechanically cutting, polishing and preparing the sample for cross-sectioning [2].

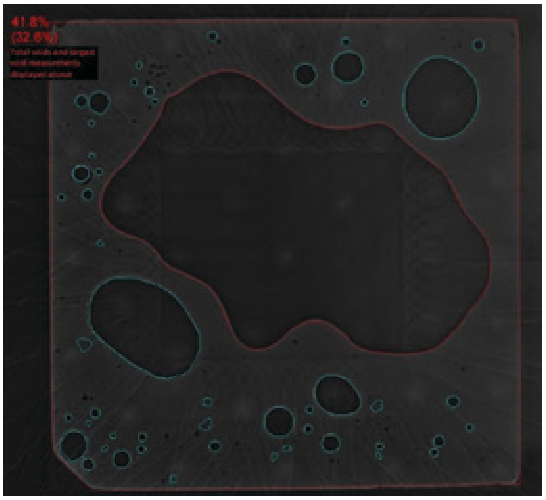

Figure 3. Large Board CT (X-plane) slice displaying void analysis. The pad layer within the QFN device have been isolated clearly revealing all voiding. Voiding has been calculated automatically and outlined in colour. The large void outlined in red measures 32.6% of the area of the QFN pad.

Large Board CT (X-plane) is a partial angle 3D computer tomography technique that works by orbiting the detector around the area of interest within the sample. During one orbit of the detector multiple images are captured, and then these images are used to reconstruct a 3D model. Figure 3 displays a single slice image focusing on the layer of voiding within the QFN device seen in figure 2. The pad layer within the QFN device have been isolated clearly revealing all voiding. Voiding has been calculated automatically and outlined in colour. All other sample layers have been virtually removed, making it easier to only study the layer of interest.

Big advantage of the Large Board CT is that it can handle extremely large samples (up to 1205 x 672 mm) in a completely non-destructive way. µCT is another 3D inspection technique where the X-ray source and detector remain fixed and the sample is rotated while multiple images are accumulated. These are further used to reconstruct the 3D model. The µCT technique is limited to smaller samples, but provides extremely high resolution. 3D rendering of a QFN device using µCT is shown on Figure 4. Large Board CT and µCT are complimentary techniques permitting in-depth 3D studies of the samples including virtual micro-sectioning used jointly to reveal the most concealed and challenging defects.

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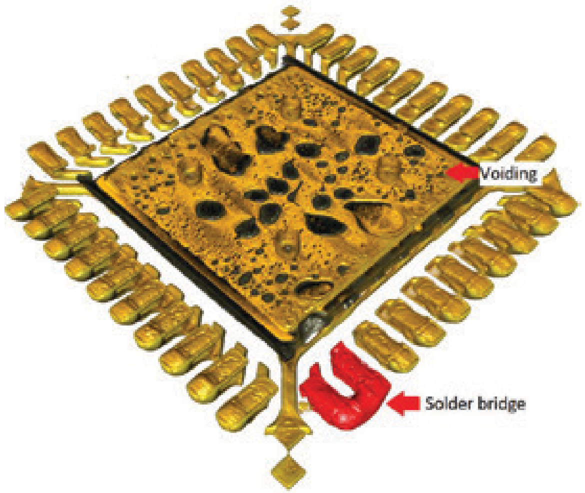

Figure 4. High resolution µCT 3D model image of a QFN displaying solder voiding and a solder bridge.

Real Time X-ray Reflow Simulator

The X-ray Reflow Simulator, is specifically designed to observe solder paste reflow in real time using live X-ray inspection. Basically, it is a small reflow oven that fits inside the X-ray machine and permits samples to be heated through pre-defined temperature profiles (Figure 5). Cover gas can also be applied to simulate inert reflow. Temperatures of up to 350^{0}C, increasing at up to 5^{0}C/ second can be programmed. A halogen bulb and a ceramic heater make it possible to simultaneously heat both the top side and underside of the sample. Thermocouples track the temperature of both heaters, and the sample. Adjustable sample rails make it easy to place both small and larger samples into the Reflow Simulator.

Figure 5. Real time X-ray Reflow Simulator.

Figure 6 shows an X-ray image captured during real time reflow of a QFN device. The solder reflow begins at 235^{0}C. At this point, voids can clearly be seen forming and after that merging into larger void formations (highlighted with a red arrow). The shape of some of the larger voids is an indication of the direction the voids are moving around the pad. The large void highlighted with a green arrow can be seen moving towards the edge of the pad, once it reaches this position, the void then outgasses. Outgassing is the process of releasing trapped air/gas within a material, in this case trapped air within solder. The best way to monitor the process is through a real-time video that is captured by the equipment. These videos are available upon request and will be presented during the talk

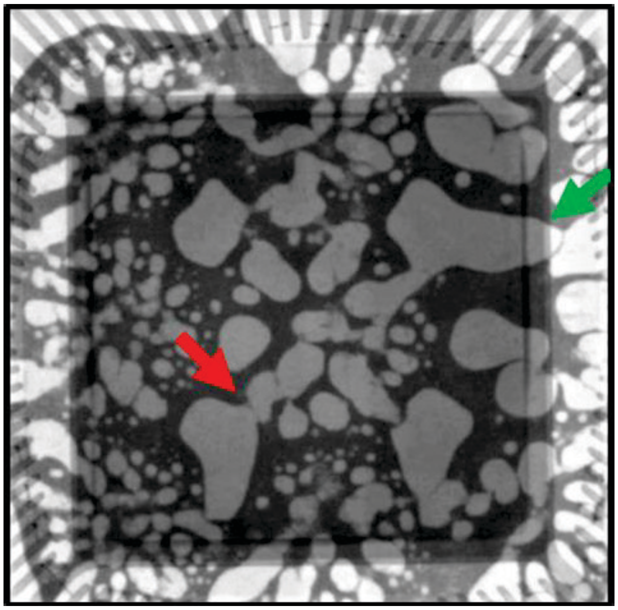

Figure 6. 2D X-ray image captured within the X-ray Reflow Simulator as solder reflow begins at 235^{0}C. Void formation and propagation can clearly be seen. The best way to monitor the process is through a real-time video that is captured by the equipment. These videos are available upon request and will be presented during the talk.

Figure 7 shows the changes in QFN void dynamics compared with figure 6 as the temperature increases from 235^{0}C to 250^{0}C. This image has been captured just before multiple voids outgas. The voids expand with the increase in temperature and eventually the trapped air is released. The red arrows are highlighting voids which are just about to outgas, displayed as a faint grey colour. Interestingly, multiple new voids are seen forming right in the same area of voids that are outgassing, displayed as a darker grey colour.

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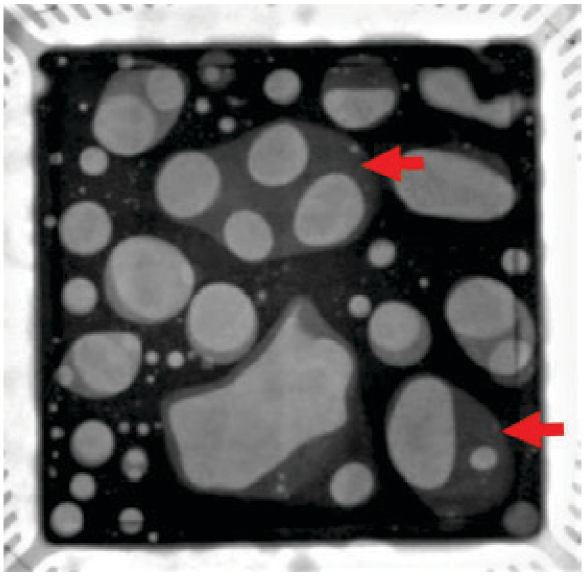

Figure 7. 2D X-ray image captured during solder reflow at 250^{0}C. Location of void outgassing and formation can clearly be seen. The red arrow shows voiding in process of outgassing. The best way to monitor the process is through a real-time video that is captured by the equipment. These videos are available upon request and will be presented during the talk.

Experimental Procedure

Figure 8 shows the PCB used within this experiment. A QFN device has been mounted on the board and all other areas have been left bare and unsoldered. The board is then placed into the Reflow Simulator, the heating profile programmed and executed. Video and still images are recorded throughout the entire process that is synchronised with the temperature readings.

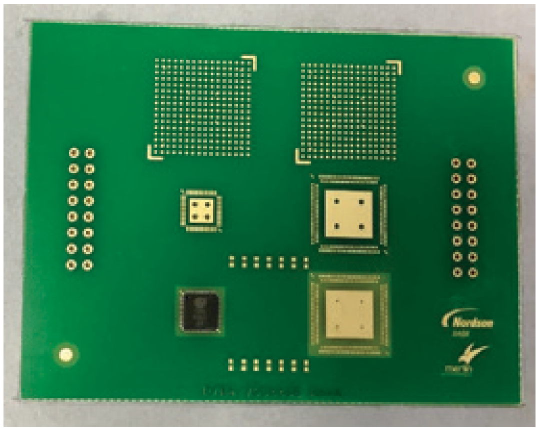

Figure 8. Test board optical mage. The voiding dynamics during reflow is studied for the QFN device located at the bottom left of the board.

Below are the test conditions and parameters:

- Identical sample boards with the same stencil design were used.
- Matching QFN components were mounted to the boards for analysis.
- Different solder pastes were used to study void formation and dynamics. All pastes are lead-free and the alloy content of the solder pastes is as below:
- Solder paste type 1 – SAC 305 – T3 (96.5% tin, 3% silver, 0.5% copper)
- Solder paste type 2 – SAC 387 – T3 (95.5% tin, 3.8% silver, 0.7% copper)
- Solder paste type 3 - SAC 305 – T3 (96.5% tin, 3% silver, 0.5% copper)
- The thermal profile used to reflow each paste was identical (Figure 9). The temperature was increased by 2^{0}C/ second to a maximum of 245^{0}C. Two hold times of 15 seconds were included at 125^{0}C and 200^{0}C

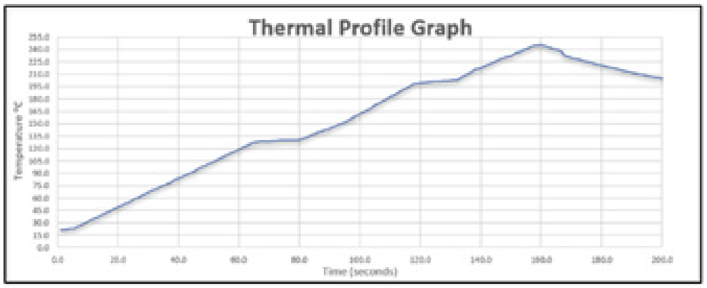

Figure 9. Thermal reflow profile used was identical for all paste types.

- Images were captured and video recorded during the solder reflow to study the void formation and outgassing dynamics.
- Further analysis was performed after reflow to characterise the final voiding levels.

Results and Discussions

The results from the experiments are discussed below.

The void dynamics formation for solder paste type 1 is shown on Figure 10. The solder starts to reflow at 235^{0}C across the pad, and at the same time void formation begins. As the temperature increases to 238^{0}C, the smaller voids merge into larger voids, particularly towards the middle of the device. At this point voids are distributed all over the pad. With temperature increasing to 245^{0}C the voids continue to move, coalesce and outgas. The large void that is seen at 238^{0}C in the centre of the pad outgasses, and a new void forms in the same location seen at 245^{0}C.

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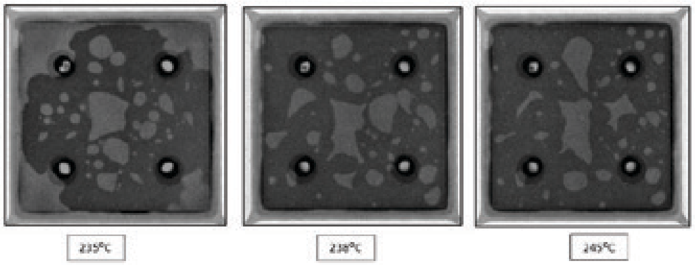

Figure 10. Void dynamics during solder paste type 1 reflow

Solder paste type 2 behaviour is seen on Figure 11. The reflow and void formation starts at 235^{0}C. With the temperature increasing to 238^{0}C smaller voids coalesce creating fewer but larger ones. With temperature further increasing to 245^{0}C the large voids move towards the edges where they outgas.

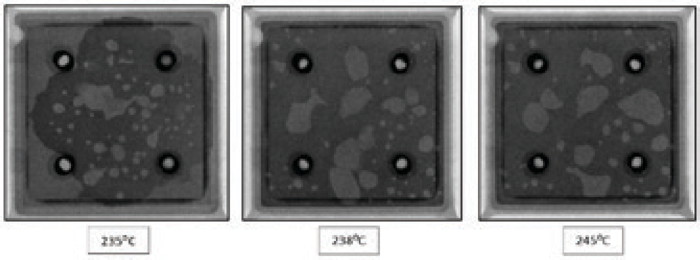

Figure 11. Void dynamics during solder paste type 2 reflow.

Solder paste type 3 also starts to reflow at 235^{0}C and at the same time multiple small voids are formed (Figure 12). The size of the voids at 238^{0}C is small to moderate and they are still concentrated in the middle of the device. With temperature increasing further to 245^{0}C additional moderate size voiding is created and the voids are distributed all around the pad. The voids outgas at the location they form contrasting the behaviour of solder paste type 2 where the large voids move towards the edges to outgas.

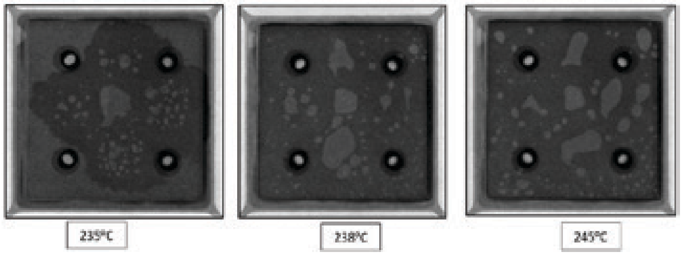

Figure 12. Void dynamics during solder paste type 3 reflow.

Summary of the void dynamics behaviour is presented in Table 1. Solder paste 1 and 3 generally displayed similar behaviour. The distribution of voids over the entire pad were wide-spread in both pastes as max reflow temperature was reached. It was observed that voiding displayed minimal movement to outgas. The voids were seen to outgas from the location they formed, and as voids outgassed, new voids would form in the same locations. The only noticeable difference seen between solder paste 1 and 3 was the size of voiding that formed. Solder paste 1 formed larger voiding compared with solder paste 2.

Summary of Void Dynamics During Real-Time Solder Reflow			
	Formation of Voids	Distribution of Voids	Outgassing of Voids
Solder Paste 1	Small to large	Wide-spread	Location formed
Solder Paste 2	Small to large	Wide-spread	Edge of pad
Solder Paste 3	Small to moderate	Wide-spread	Location formed

Table 1. Summary of Void Dynamics During Real-Time Solder Reflow.

Solder paste 2 showed similarities to the other pastes in formation and distribution of voids, but displayed a distinct outgassing behaviour. As the smaller voids formed into larger voids, these larger voids then slowly moved towards the edge of the pad and then outgassed. Once the large void outgassed, the process of smaller voids collating and forming larger voids would repeat. Area void calculations were performed for all 3 cases after reflow and cooldown. The results are presented on Figure 13.

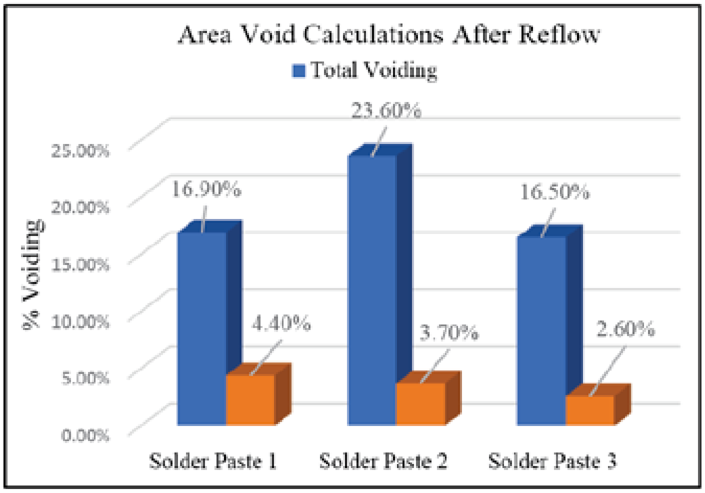

Figure 13. Area voiding calculations after reflow for the 3 paste types.

Solder pastes 1 and 3 show similar total voiding, between 16% and 17%, while the total voiding of solder paste 2 is much higher at 23.6%. This could be attributed on the different voiding dynamics behaviour as discussed in Table

1. To explore the validity of this hypothesis a much larger sample size is needed so one can build the proper statistics. We plan to perform such a study in a near future.

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Conclusion

In this paper we presented the real time X-ray reflow simulator. This clever device is basically a miniature reflow oven that fits inside the real time X-ray inspection system and permits the solder reflow process of QFN and BGA devices to be viewed in real time and recorded. A case study was also presented comparing the behaviour of 3 different solder pastes. Correlation between reflow behaviour and final total voiding was suggested. Much larger study is necessary to build the proper statistics and further test this hypothesis.

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